What is claimed is:

1. A semiconductor memory device comprising:

a memory cell array having a plurality of data select lines disposed in parallel with each other, a plurality of data transfer line disposed in parallel with each other to intersect said data select lines, and electrically rewritable memory cells laid out at cross portions between said data select lines and data transfer lines;

a data select line driver for driving said data select lines of said memory cell array;

a sense amplifier circuit connected to said data transfer lines of said memory cell array, for performing data read of memory cells selected by one of said data select lines; and

a control circuit used for timing control of data read of said memory cell array, for outputting at least two types of timing signals as being different in accordance with a selected data area of said memory cell array.

2. The semiconductor memory device according to claim 1, wherein

said memory cell array is divided into at least one first area and at least one second area in the direction of said data select lines in such a way that these areas are simultaneously selected by one of said data select lines, and wherein

said control circuit has a first timing circuit for outputting a timing signal necessary for performing data read of said first and second areas simultaneously selected by one of said data select lines within a first cycle time and a second timing circuit for outputting a timing signal necessary for performing selective data read of said second area within a second cycle time shorter than said first cycle time.

3. The semiconductor memory device according to claim 2, wherein

said memory cell array is divided into a plurality of

cell blocks in the direction of said data transfer lines, each said cell block including plural data select lines.

4. The semiconductor memory device according to claim 3, wherein

said memory cell array is divided into a first area and a second area in the direction of said data select lines in a way that these areas are simultaneously selected by one of said data select lines, and wherein

said data select line driver is disposed at an end portion of said data select lines in close proximity to said second area.

5. The semiconductor memory device according to claim 3, wherein

said memory cell array is divided into at least two first areas and at least one second area interposed between said first areas in the direction of said data select lines in a way that these areas are simultaneously selected by one of said data select lines, and wherein

said data select line driver includes parts alternately disposed at opposite end portions of said data select lines in units of said cell blocks.

6. The semiconductor memory device according to claim 3, wherein

said memory cell array is divided into at least one first area and at least two second areas laid out on opposite sides of said first area in the direction of said data select lines in a way that these areas are simultaneously selected by one of said data select lines, and wherein

said data select line driver includes parts alternately disposed at opposite end portions of said data select lines in units of said cell blocks.

7. The semiconductor memory device according to claim 3, wherein

each said cell block includes NAND type cell units each having a plurality of memory cells connected in series

and driven by different data select lines respectively and a select gate transistor with at least one end thereof being connected to a corresponding data transfer line.

8. The semiconductor memory device according to claim 3, wherein

each said cell block includes AND type or virtual ground type cell units each having a plurality of memory cells connected in parallel and driven by different data select lines respectively and a select gate transistor with at least one end thereof being connected to a corresponding data transfer line.

9. The semiconductor memory device according to claim 1, wherein

said device has at least two data read modes with different minimum cycle times necessary for continuously read out plural columns of said memory cell array.

10. The semiconductor memory device according to claim 1, wherein

said device has a data write mode for writing data into selected memory cells, said data write mode including a verify-read operation for verifying a write state.

11. The semiconductor memory device according to claim 2, further comprising:

an error bit correction circuit for performing error correction of at least one bit of data read into said sense amplifier circuit.

12. The semiconductor memory device according to claim 2, wherein

said second area serves as at least one of a memory cell area for replacement of a memory cell in said first area, an ECC record area for recording an error correction code of data to be written into said first area, and a flag area for storing a full erase state and/or a write state of said first area.

13. The semiconductor memory device according to claim 4, further comprising:

a verify check circuit for determining write completion of all write data based on the data read out to said sense amplifier circuit during verify-read in a data write cycle.

14. The semiconductor memory device according to claim 5, further comprising:

an initial setting data storage circuit for storing therein a column address;

a column address match detecting circuit for performing detection of coincidence of an input column address to the column address stored in said initial setting data storage circuit; and

a column address conversion circuit for performing, based on an output of said column address match detecting circuit, address conversion for replacing a defective column of said first area with a column of said second area.

15. The semiconductor memory device according to claim 14, wherein

said logical/physical address conversion circuit has an inverter for inverting an uppermost bit of logical column address.

16. The semiconductor memory device according to claim 11, wherein

the number of data bits "n" to be read or written via an input/output port satisfying a relationship of $2^{m-1}-m<n\leqq 2^{m}-m-1$ (where, "m" is a natural number), at least (n+m) memory cells are laid out in the direction of said data select lines.

17. A file system comprising said semiconductor memory device according to claim 1, wherein

after data write into a certain area, a write completion flag as to the certain area is written simultaneously during data write to another area.

18. A file system comprising said semiconductor memory device according to claim 1, wherein

data rewrite after data write has been interrupted due

to power supply stopping is performed within a time shorter than normal data write after data erasure.

19. A semiconductor memory device comprising:

a memory cell array having a plurality of data select lines disposed in parallel with each other, a plurality of data transfer line disposed in parallel with each other to intersect said data select lines, and electrically rewritable memory cells laid out at cross portions between said data select lines and data transfer lines;

a data select line driver for driving said data select lines of said memory cell array;

a sense amplifier circuit connected to said data transfer lines of said memory cell array, for performing data read of memory cells selected by one of said data select lines; and

a logical/physical address conversion circuit for exchanging an order of at least part of physical addresses to be sequentially selected by input logical addresses, address output thereof being input to said sense amplifier circuit.

20. The semiconductor memory device according to claim 19, wherein

said memory cell array is divided into a plurality of cell blocks in the direction of said data transfer lines, each said cell block including plural data select lines.

21. The semiconductor memory device according to claim 20, wherein

each said cell block includes NAND type cell units each having a plurality of memory cells connected in series and driven by different data select lines respectively and a select gate transistor with at least one end thereof being connected to a corresponding data transfer line.

22. The semiconductor memory device according to claim 20, wherein

each said cell block includes AND type or virtual ground type cell units each having a plurality of memory

cells connected in parallel and driven by different data select lines respectively and a select gate transistor with at least one end thereof being connected to a corresponding data transfer line.

23. The semiconductor memory device according to claim 20, further comprising:

an error bit correction circuit for performing error correction of at least one bit of data read into said sense amplifier circuit.

24. The semiconductor memory device according to claim 23, wherein

said logical/physical address conversion circuit exchanges, in a data read mode continuously reads out plural columns of said memory cell array, an order of at least part of logical addresses and physical addresses of an ECC record area for recording an error correction code of data.

25. The semiconductor memory device according to claim 20, wherein

said memory cell array is divided in the direction of said data select lines into two first areas and a second area interposed between said first areas in a way that these areas are simultaneously selected by one of said data select lines, said second area serving as a memory cell area for replacement of a column in said first areas and an ECC record area for recording an error correction code of data to be written into said first areas, and wherein

said data select line driver includes components alternately disposed at opposite end portions of said data select lines in units of said cell blocks, and wherein

said device further comprises a control circuit having a first timing circuit for outputting a timing signal necessary for reading memory cells of said first and second areas simultaneously selected by one of said data select lines within a first cycle time and a second timing circuit for outputting a timing signal necessary for performing

selective data read of said second area within a second cycle time shorter than said first cycle time.

26. The semiconductor memory device according to claim 25, further comprising:

an initial setting data storage circuit for storing therein a column address;

a column address match detecting circuit for performing detection of coincidence of an input column address to the column address stored in said initial setting data storage circuit; and

a column address conversion circuit for performing, based on an output of said column address match detecting circuit, address conversion for replacing a defective column of said first areas with a column of said second area.

27. The semiconductor memory device according to claim 26, wherein

said logical/physical address conversion circuit has an inverter for inverting an uppermost bit of logical column address.

28. The semiconductor memory device according to claim 19, wherein

the number of data bits "n" to be read or written via an input/output port satisfying a relationship of $2^{m-1}-m<n\leqq 2^{m}-m-1$ (where, "m" is a natural number), at least (n+m) memory cells are laid out in the direction of said data select lines.

29. A file system comprising said semiconductor memory device according to claim 19, wherein

after data write into a certain area, a write completion flag as to the certain area is written simultaneously during data write to another area.

30. A file system comprising said semiconductor memory device according to claim 19, wherein

data rewrite after data write has been interrupted due to power supply stopping is performed within a time shorter

than normal data write after data erasure.